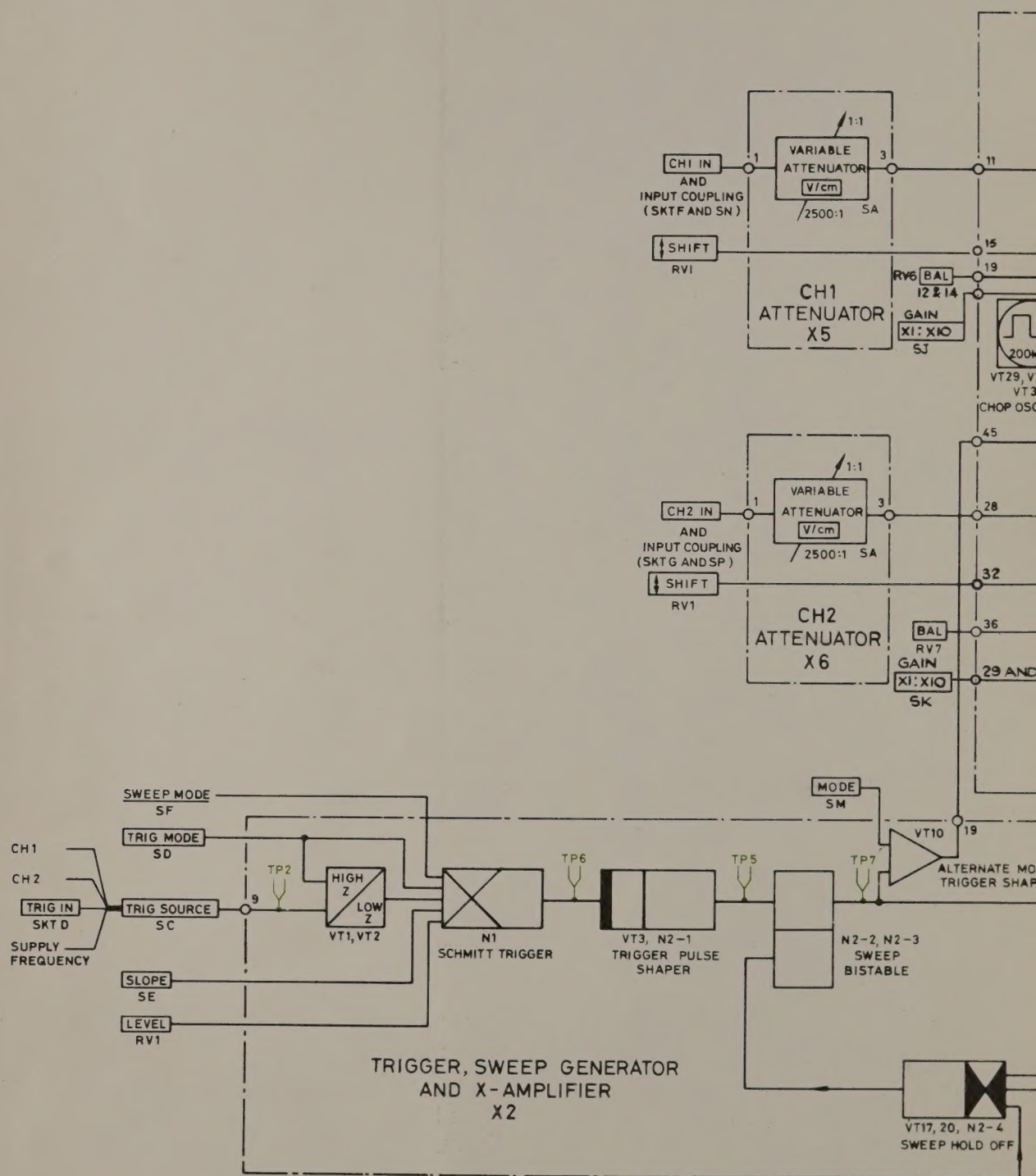
351

mi

TF2204

18 MHz Oscilloscope

MARCONI INSTRUMENTS LIMITED


CH1 IN
AND
INPUT COUPLING
(SKT F AND SN)
1:1
VARIABLE
ATTENUATOR
V/cm
2500:1
SA
SHIFT
RV1
CH1
ATTENUATOR
X5
RV6
BAL
12 & 14
GAIN
X1 : X10
SJ
CHOP OSC
CH2 IN
AND
INPUT COUPLING
(SKT G AND SP)
SHIFT
RV1
CH2
ATTENUATOR
X6
BAL
RV7
GAIN
X1 : X10
SK
SWEEP MODE
SF
TRIG MODE
SD
CH1
CH2
TRIG IN
SKT D
TRIG SOURCE
SC
SUPPLY
FREQUENCY
SLOPE
SE
LEVEL
RV1
TP2
HIGH Z
LOW Z
VT1, VT2
N1
SCHMITT TRIGGER
TP6
VT3, N2-1
TRIGGER PULSE
SHAPER
TP5
TP7
N2-2, N2-3
SWEEP
BISTABLE
MODE
SM
VT10
ALTERNATE MO
TRIGGER SHAP
TRIGGER, SWEEP GENERATOR
AND X-AMPLIFIER
X2
VT17, 20, N2-4
SWEEP HOLD OFF

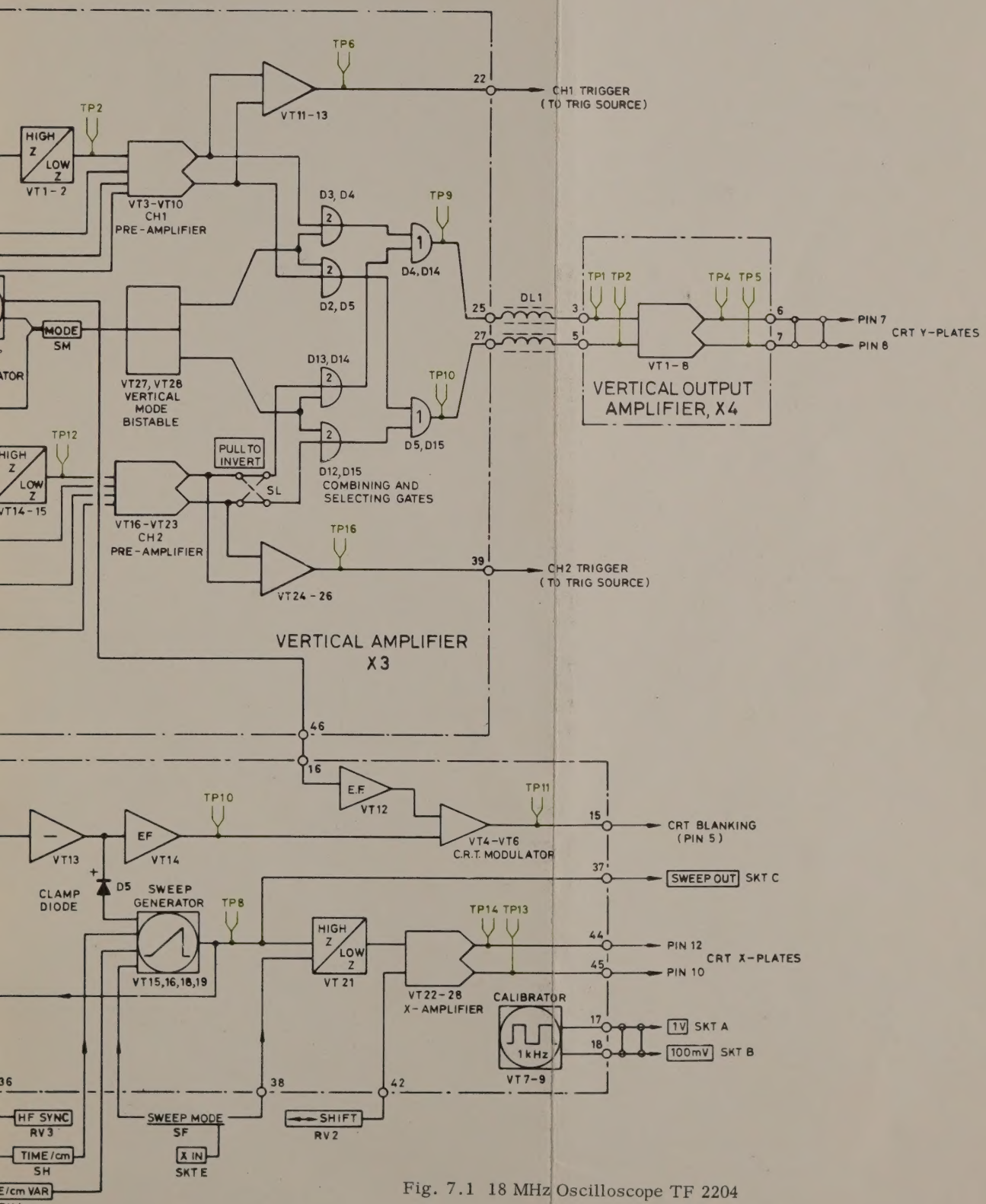
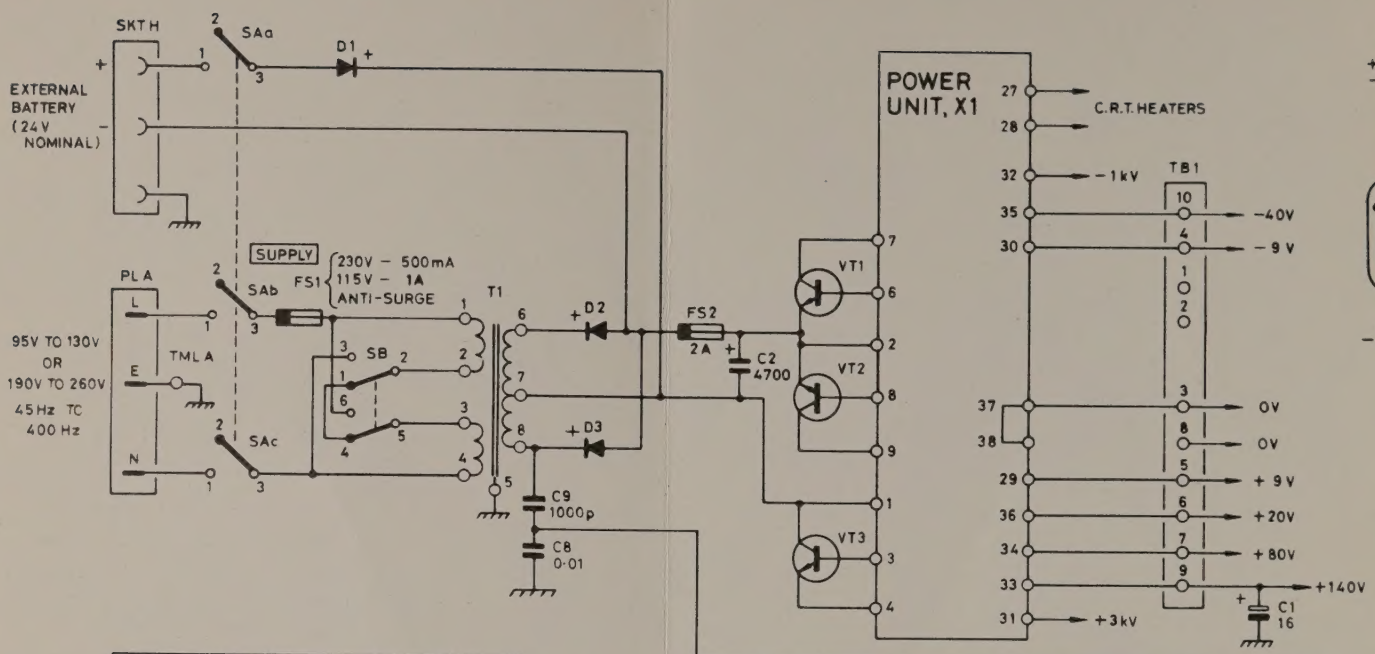
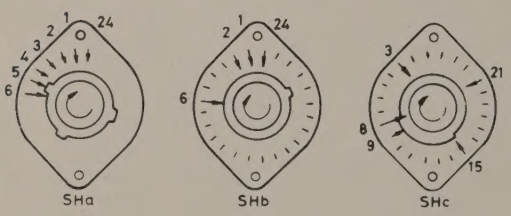


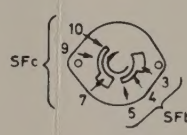
Fig. 7.1 18 MHz Oscilloscope TF 2204



TIME/cm RANGE SELECTED		WAFER CONTACTS MADE					
		SHa	SHb	SHc	SHd	SHe	SHf
1		5	–	9	10	9	10
0·5	S	4	–	9	10	9	10
0·2		3	–	9	10	9	10
0·1		2	–	9	10	6	10
50		1	–	9	10	6	10
20		24	–	9	10	6	10
10		5	–	3	4	3	4
5		4	–	3	4	3	4
2	ms	3	–	3	4	3	4
1		2	–	3	4	24	4
0·5		1	–	3	4	24	4
0·2		24	–	3	4	24	4
0·1		5	–	21	22	21	22
50		4	–	21	22	21	22
20		3	–	21	22	21	22
10		2	–	21	22	18	22
5		1	–	21	22	18	22
2	µs	24	–	21	22	18	22
1		–	2	15	16	–	16
0·5		–	1	15	16	–	16
0·2		–	24	15	16	–	16

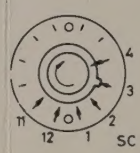


TIME/cm SWITCH: WAFERS VIEWED FROM FRONT OF SWITCH IN EXTREME COUNTER-CLOCKWISE POSITION (1 s/cm); LOCATION OF WAFERS ; TABLE OF CONTACTS MADE.



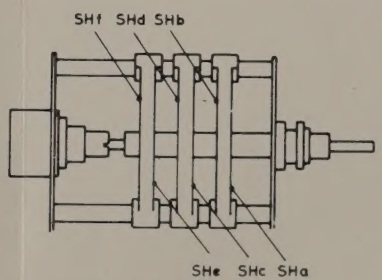
MODE SELECTED	WAFER CONTACTS MADE		
	SFa	SFb	SFc
INT	3	5	9
EXT AC	2	3	7
EXT DC	1	3	7

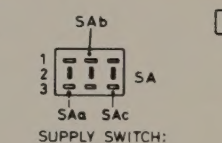
SWEEP MODE SWITCH : WAFERS AND ROTORS VIEWED FROM ARROW 'A' (LEVER IN EXT DC POSITION)



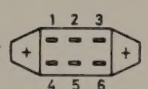
TRIGGER SOURCE SELECTED	WAFER CONTACT MADE
SUPPLY FREQ.	3
EXT ÷ 20	2
EXT	1
CH2	12
CH1	11

TRIGGER SOURCE SWITCH: WAFER AND ROTOR VIEWED FROM FRONT OF SWITCH IN EXTREME COUNTER-CLOCKWISE POSITION (SUPPLY FREQ)



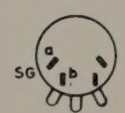


SUPPLY SWITCH: VIEWED FROM REAR OF FRONT PANEL



SUPPLY SELECTOR SWITCH: VIEW ON INSIDE OF REAR PANEL

TRIGGER SLOPE SWITCH: VIEWED FROM REAR OF FRONT PANEL



SWEEP X1 X5 GAIN SWITCH: VIEW ON REAR OF RV4

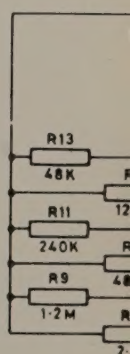
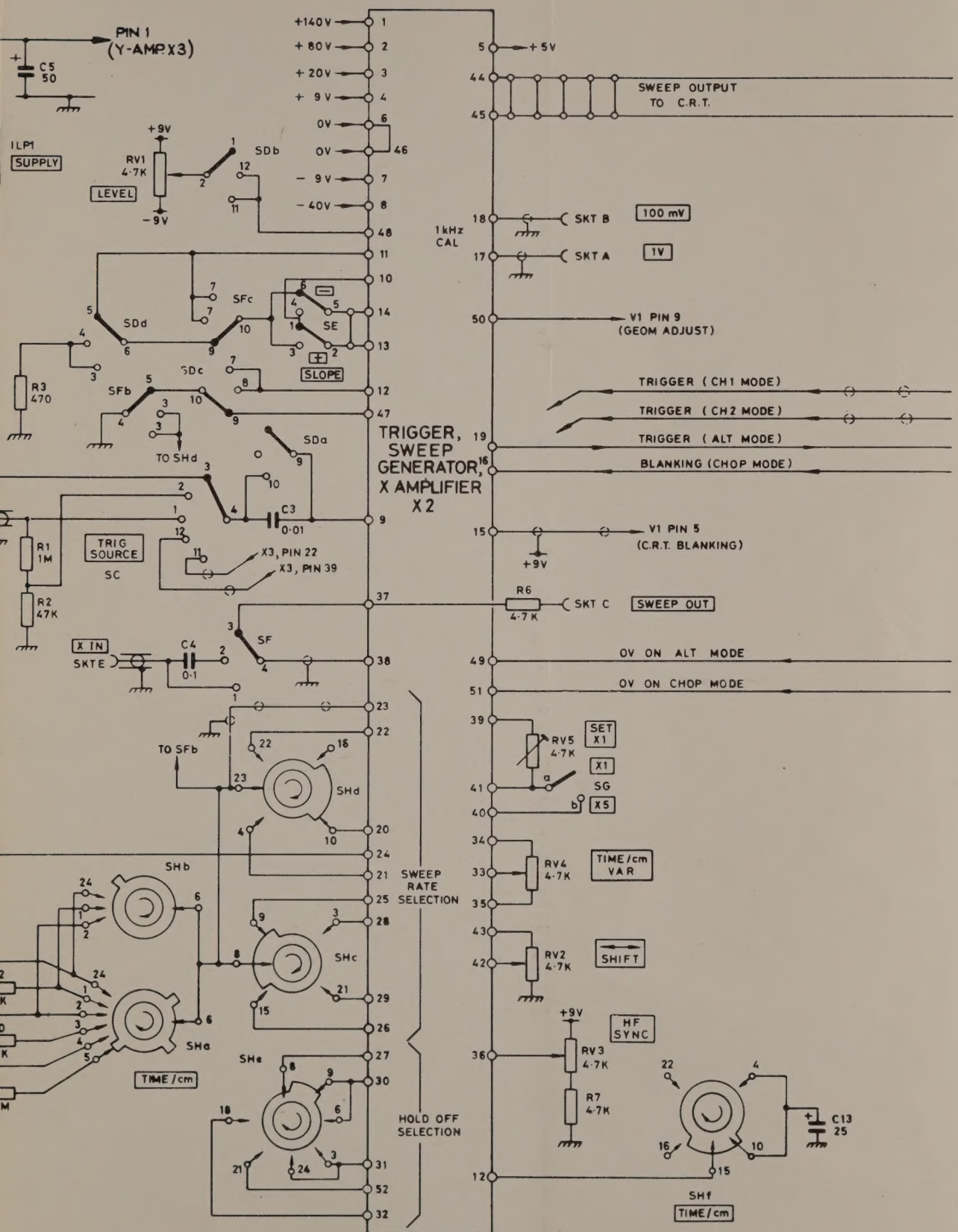
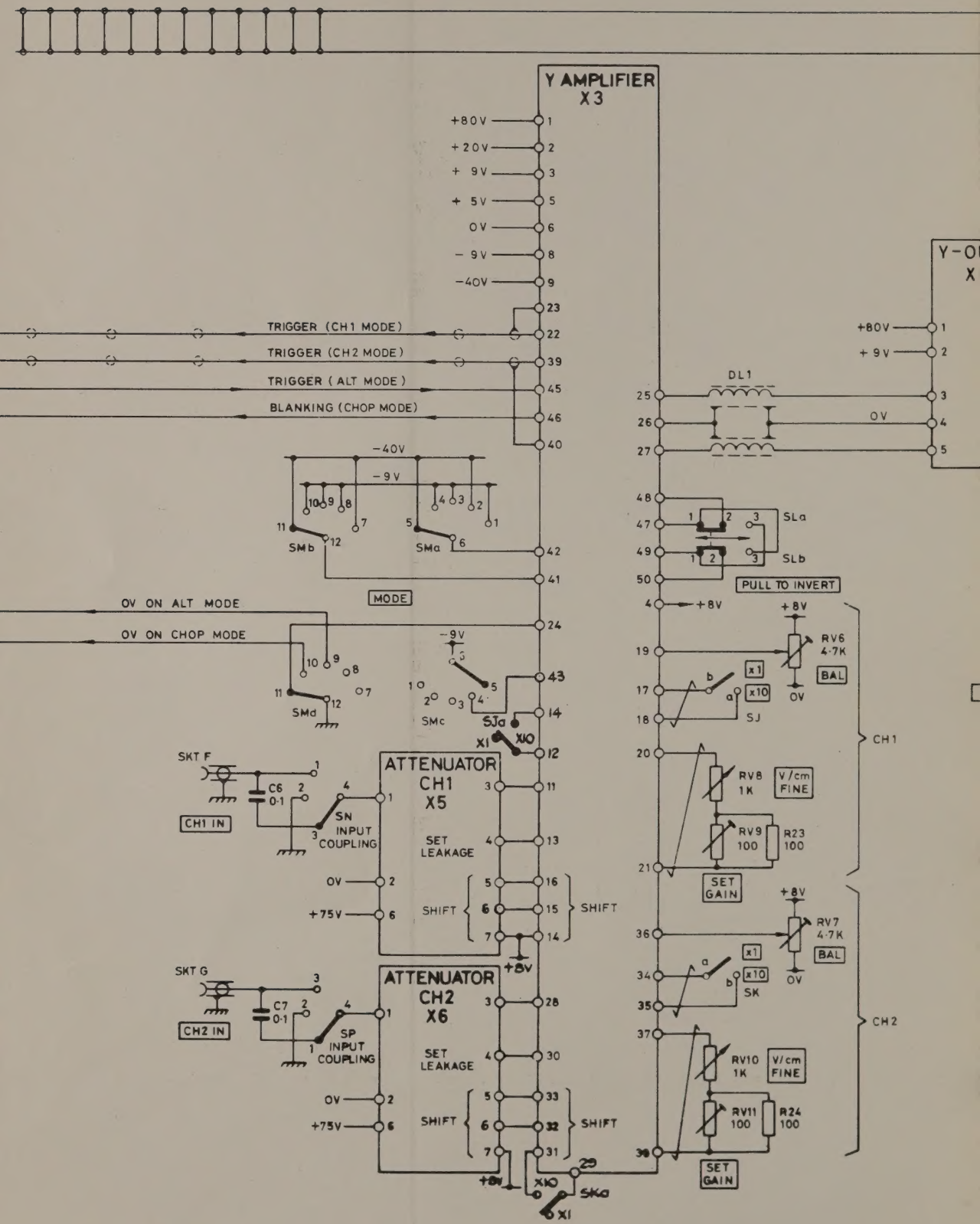
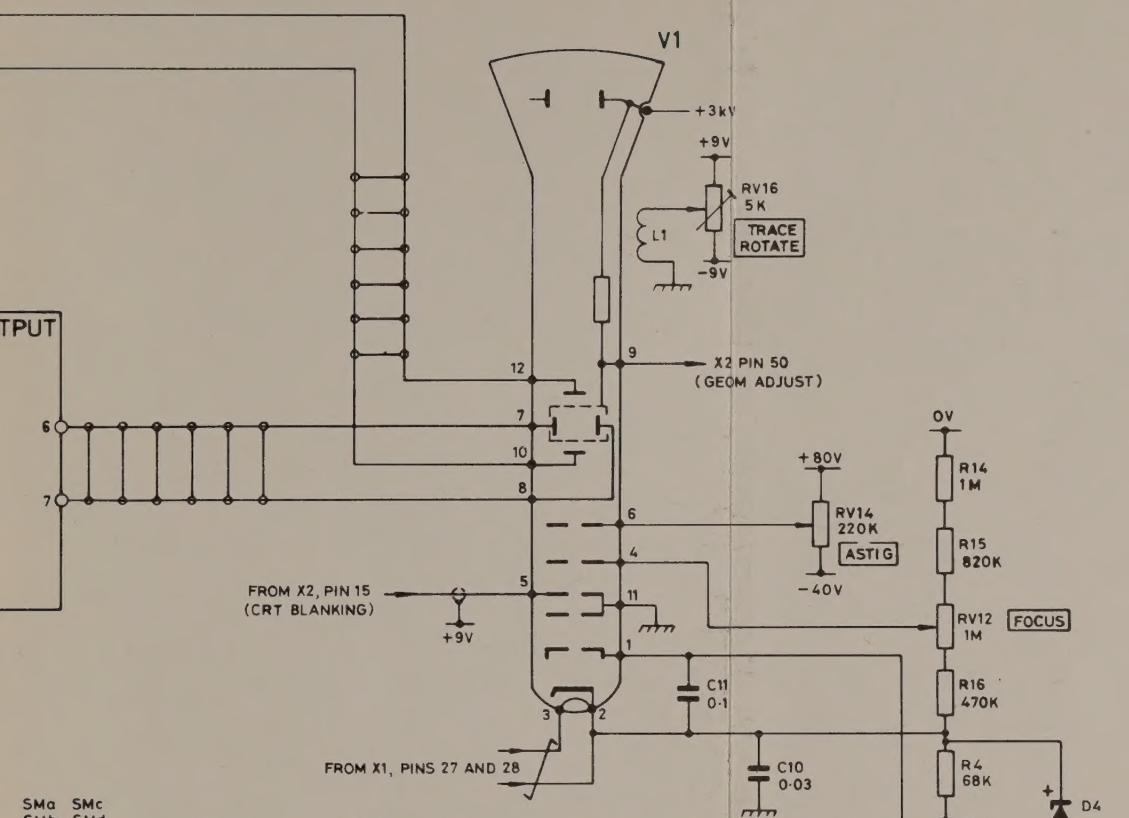
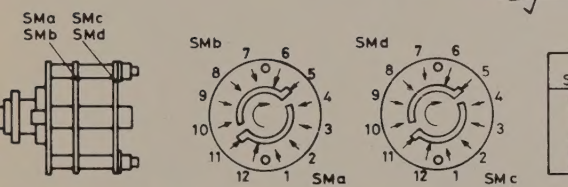


Fig. 7.2 Inter-Unit Wiring (Sheet 1)


PIN 1
(Y-AMP X3)
C5
50
ILP1
SUPPLY
+9V
RV1
4·7K
LEVEL
-9V
SDb
+140V
+80V
+20V
+9V
0V
0V
-9V
-40V
1
2
3
4
6
46
7
8
48
12
11
1kHz
CAL
18
17
SKT B
SKT A
100 mV
1V
5
+5V
44
45
SWEEP OUTPUT
TO C.R.T.
50
V1 PIN 9
(GEOM ADJUST)
SDd
SFc
SE
SLOPE
SDc
SFb
TO SHd
SDa
R3
470
TRIGGER (CH1 MODE)
TRIGGER (CH2 MODE)
TRIGGER (ALT MODE)
BLANKING (CHOP MODE)
19
16
TRIGGER,
SWEEP
GENERATOR,
X AMPLIFIER
X2
C3
0·01
R1
1M
TRIG
SOURCE
SC
R2
47K
X3, PIN 22
X3, PIN 39
15
V1 PIN 5
(C.R.T. BLANKING)
+9V
37
R6
4·7K
SKT C
SWEEP OUT
X IN
SKTE
C4
0·1
SF
38
49
OV ON ALT MODE
51
OV ON CHOP MODE
23
22
39
RV5
4·7K
SET
X1
X1
SG
X5
41
40
TO SFb
SHd
20
24
34
SHb
21
SWEEP
RATE
SELECTION
25
28
33
RV4
4·7K
TIME/cm
VAR
35
43
SHc
RV2
4·7K
SHIFT
42
29
SHa
TIME/cm
26
+9V
HF
SYNC
36
RV3
4·7K
R7
4·7K
27
SHe
30
HOLD OFF
SELECTION
C13
25
31
52
32
12
SHf
TIME/cm

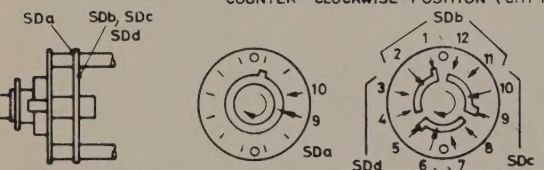

Y AMPLIFIER
X3
+80V
+20V
+ 9V
+ 5V
0V
- 9V
-40V
TRIGGER (CH1 MODE)
TRIGGER (CH2 MODE)
TRIGGER (ALT MODE)
BLANKING (CHOP MODE)
SMb
SMa
MODE
OV ON ALT MODE
OV ON CHOP MODE
SMd
SMc
SJa
X1
X10
SKT F
CH1 IN
C6 0·1
SN INPUT COUPLING
ATTENUATOR CH1 X5
SET LEAKAGE
SHIFT
SKT G
CH2 IN
C7 0·1
SP INPUT COUPLING
ATTENUATOR CH2 X6
SKa
DL1
SLa
SLb
PULL TO INVERT
RV6 4·7K
BAL
SJ
RV8 1K
V/cm FINE
RV9 100
R23 100
SET GAIN
CH1
RV7 4·7K
SK
RV10 1K
RV11 100
R24 100
CH2
Y-O
X





MODE SELECTED	WAFER CONTACTS MADE			
	SMa	SMb	SMc	SMd
CH1 + 2	5	11	5	11
CHOP	4	10	4	10
ALT	3	9	3	9
CH2	2	8	2	8
CH1	1	7	1	7

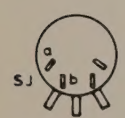
VERTICAL MODE SWITCH : WAFERS AND ROTORS VIEWED FROM FRONT OF SWITCH IN EXTREME COUNTER-CLOCKWISE POSITION (CH1 + 2)



MODE SELECTED	WAFER CONTACTS MADE			
	SDa	SDb	SDc	SDd
AUTO	–	1	9	5
AC	–	12	8	4
DC	10	11	7	3

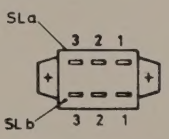
TRIGGER MODE SWITCH : WAFERS AND ROTORS VIEWED FROM FRONT OF SWITCH IN EXTREME COUNTER-CLOCKWISE POSITION

CHANNEL 2 INPUT COUPLING SWITCH: WAFER VIEWED FROM ARROW 'A' (LEVER IN AC POSITION)

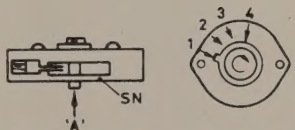


HANNEL 1 x1 x10 GAIN WITCH: VIEW ON REAR OF RV8

CHANNEL 2 x1 x10 GAIN SWITCH: VIEW ON REAR OF RV10



CHANNEL 2 PULL-TO-INVERT SWITCH: VIEW ON RIGHT HAND SIDE OF UNIT



CHANNEL 1 INPUT COUPLING SWITCH: WAFER VIEWED FROM ARROW 'A' (LEVER IN DC POSITION)

Fig. 7.2 Inter-Unit Wiring (Sheet 2)

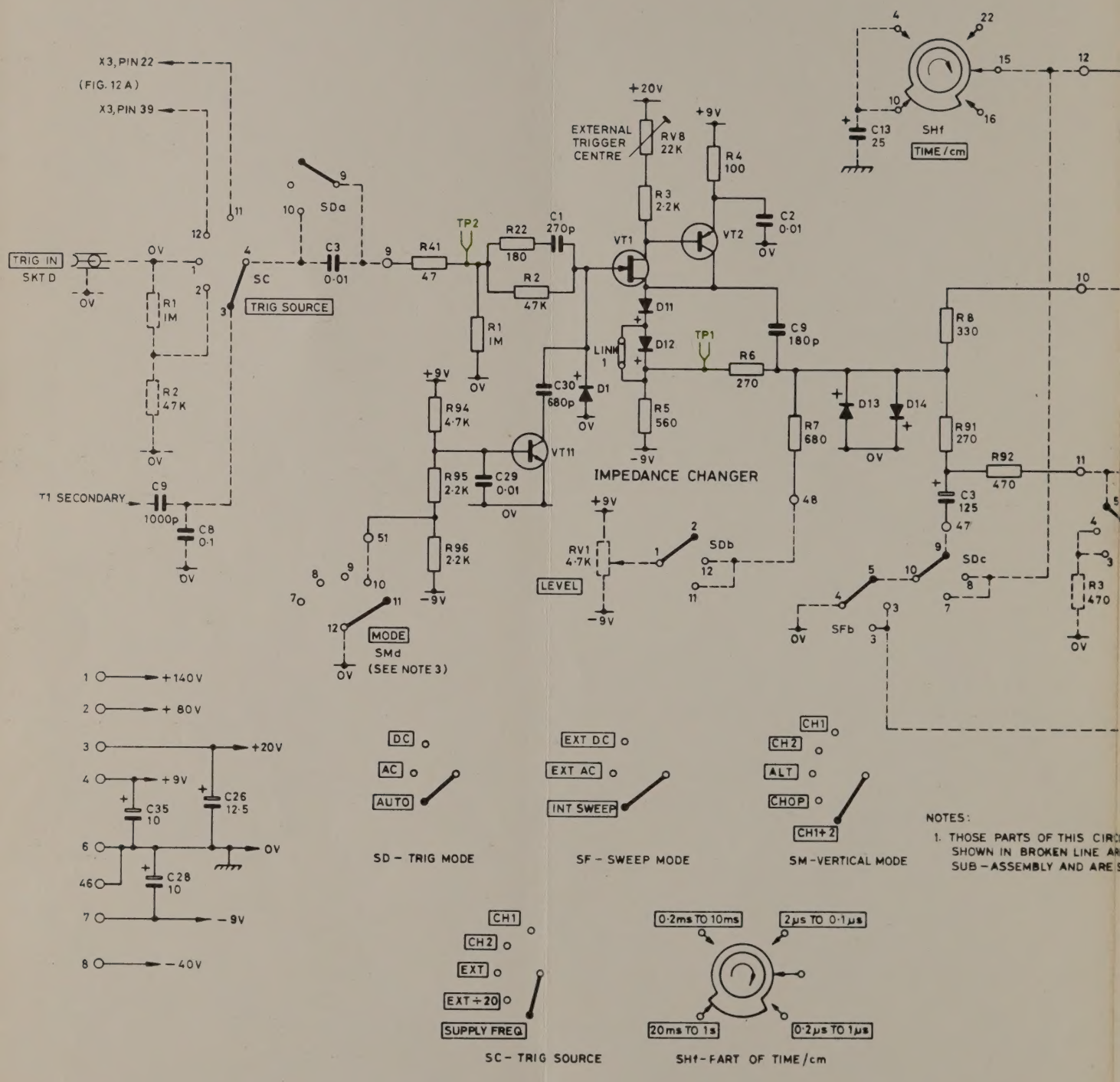
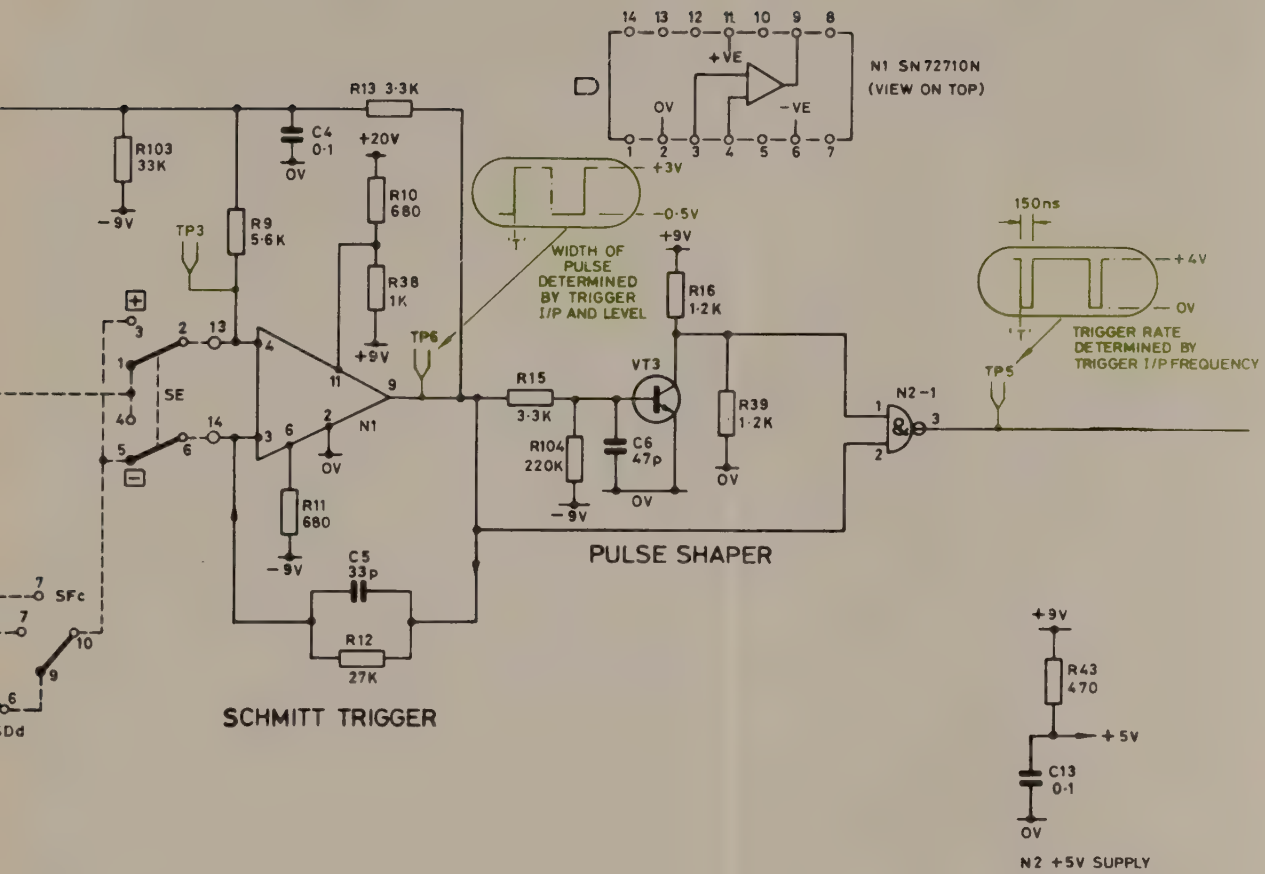
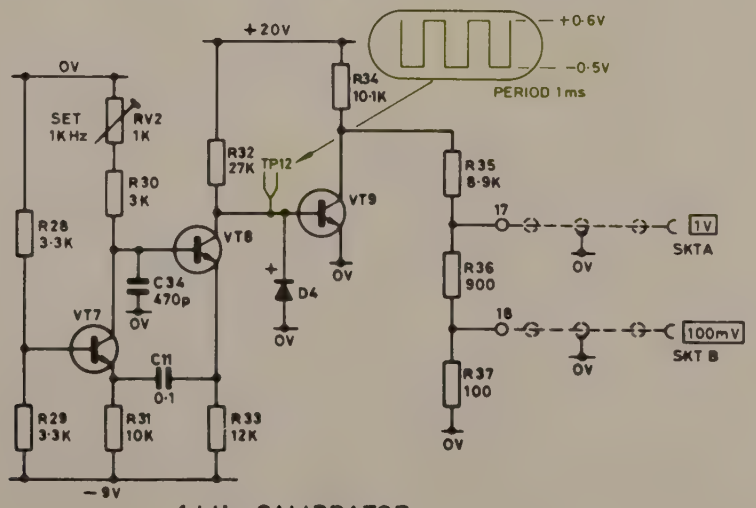
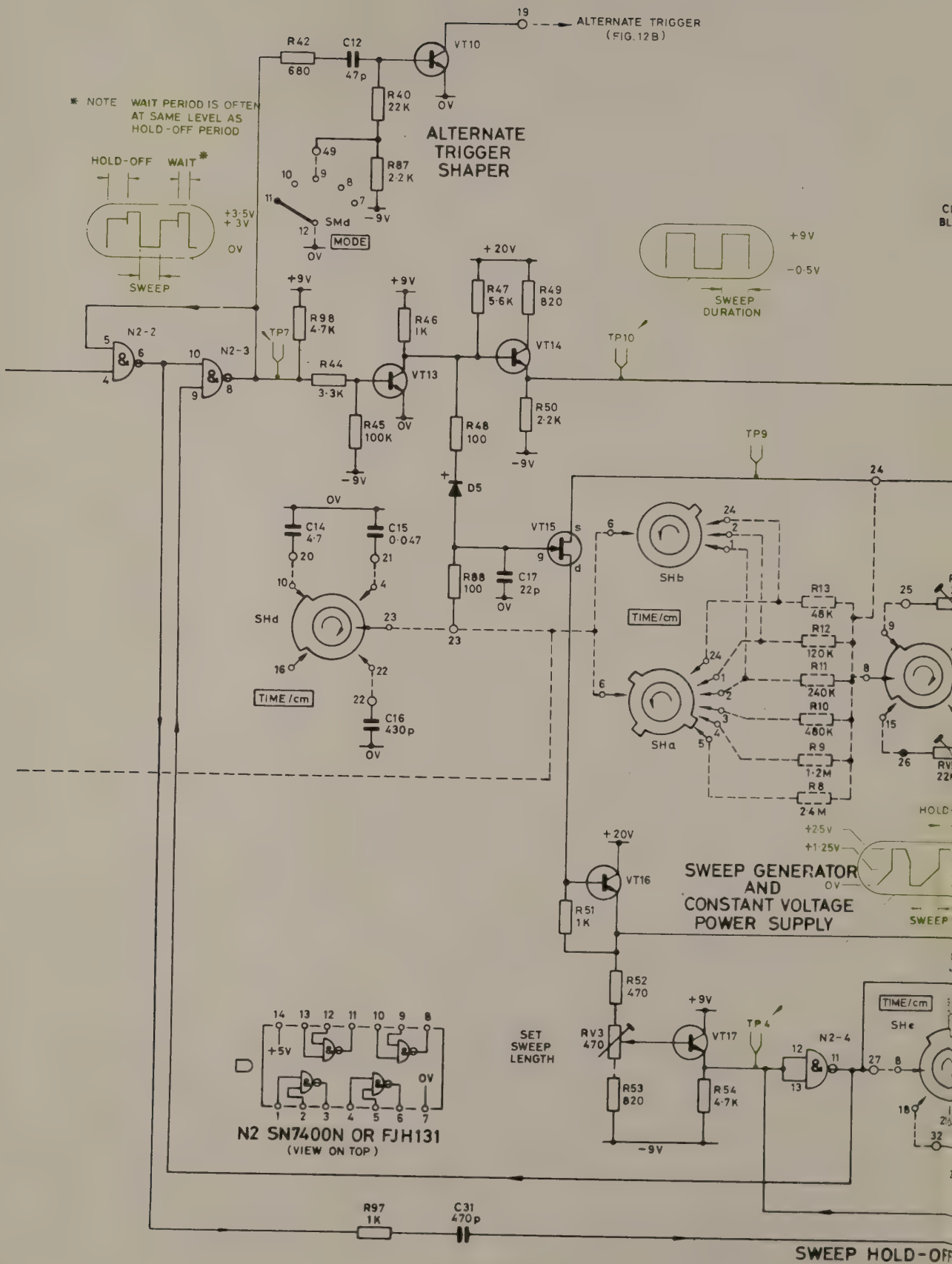


Fig. 7.3 Trigger and Sweep Generator X2 (Trigger and Calibration) Circuit Diagram



IT DIAGRAM WHICH ARE
NOT PART OF THIS
HOWN FOR CLARITY ONLY.




ALTERNATE TRIGGER (FIG. 12B)
* NOTE WAIT PERIOD IS OFTEN AT SAME LEVEL AS HOLD-OFF PERIOD
HOLD-OFF
WAIT *
SWEEP
ALTERNATE TRIGGER SHAPER
MODE
SWEEP DURATION
SWEEP GENERATOR AND CONSTANT VOLTAGE POWER SUPPLY
SET SWEEP LENGTH
TIME/cm
N2 SN7400N OR FJH131
(VIEW ON TOP)
SWEEP HOLD-OFF

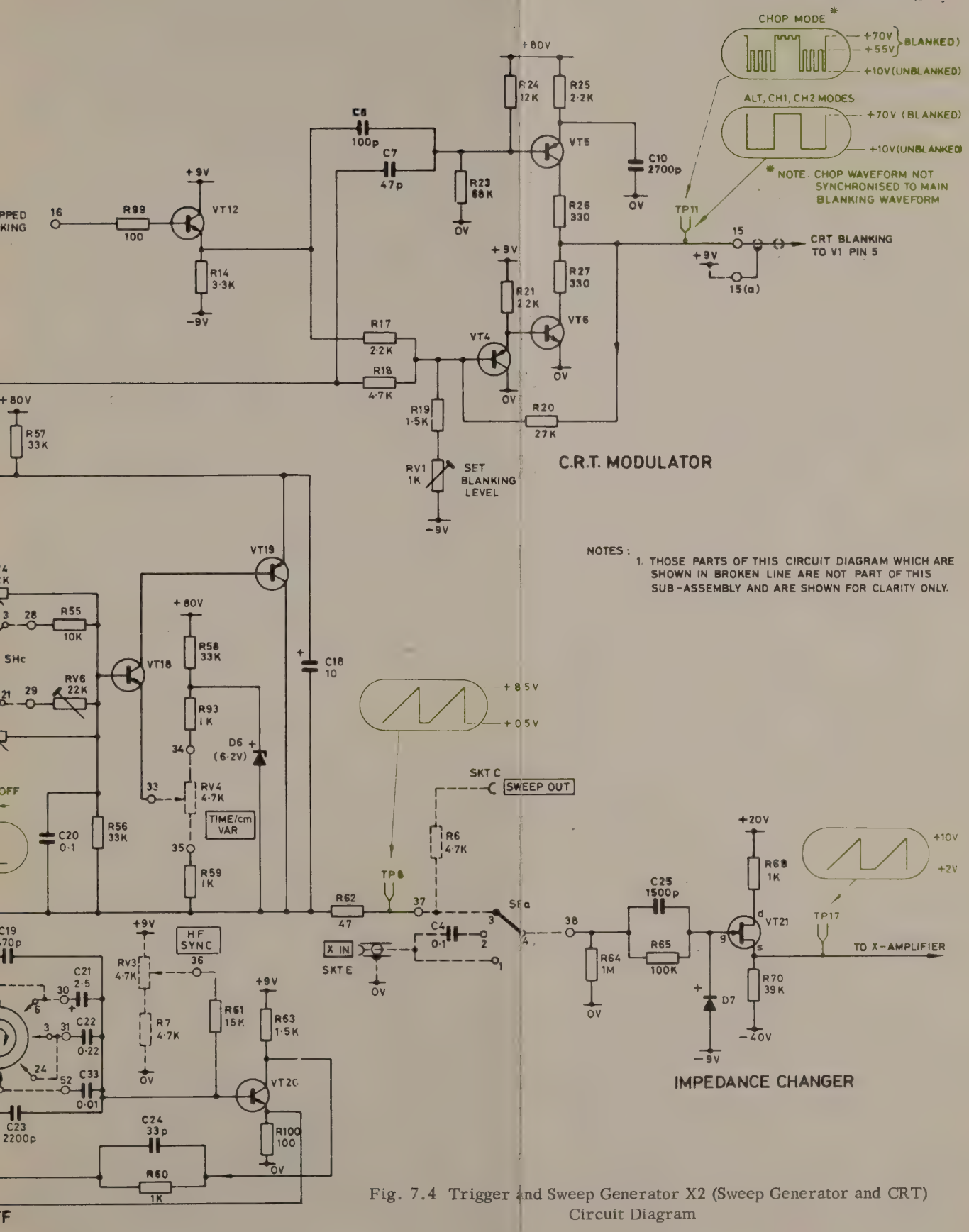


Fig. 7.4 Trigger and Sweep Generator X2 (Sweep Generator and CRT) Circuit Diagram

NOTES:

1. THOSE PARTS OF THIS CIRCUIT DIAGRAM WHICH ARE SHOWN IN BROKEN LINE ARE NOT PART OF THIS SUB-ASSEMBLY AND ARE SHOWN FOR CLARITY ONLY.

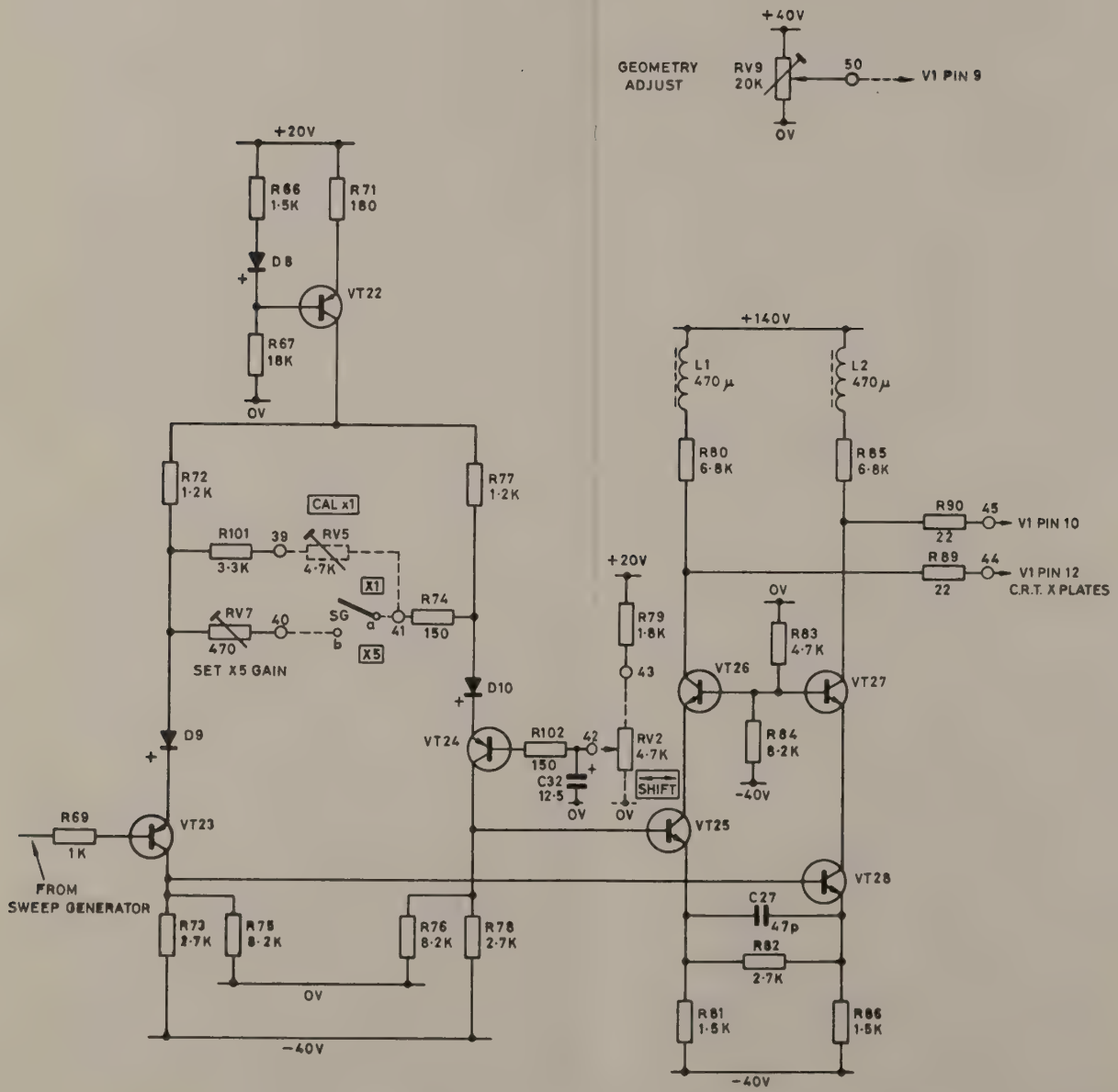
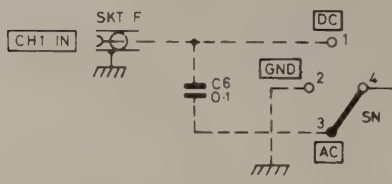


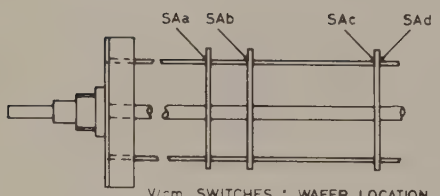
Fig. 7.5 Trigger and Sweep Generator X2 - X Amplifier Circuit Diagram

NOTES. 1. THOSE PARTS OF THIS CIRCUIT DIAGRAM WHICH ARE SHOWN IN BROKEN LINE ARE NOT PART OF THESE SUB-ASSEMBLIES AND ARE SHOWN FOR CLARITY ONLY.

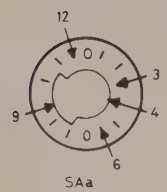
2. TAG LOCATION DIAGRAMS OF SWITCHES SN AND SP ARE SHOWN ON FIG. 7.2/2

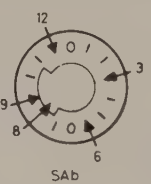
3. 5RV1 AND 6RV1 ARE ALSO SHOWN, FOR CLARITY, ON THE CIRCUIT DIAGRAM OF THE VERTICAL AMPLIFIER, X3 (CH1 AND CH2 PRE-AMPLIFIERS)



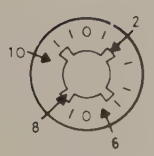


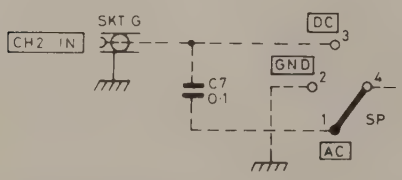
V/cm SWITCHES : WAFER LOCATION DIAGRAM





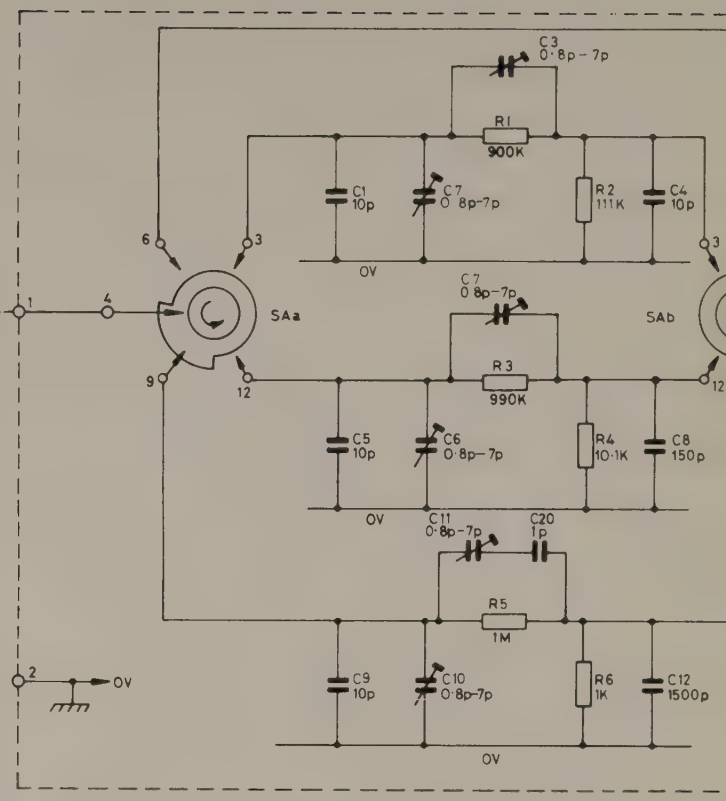
V/cm. SWITCHES WAFERS VIEWED FROM FRONT OF SWITCHES IN EXTREME COUNTER-CLOCKWISE POSITION

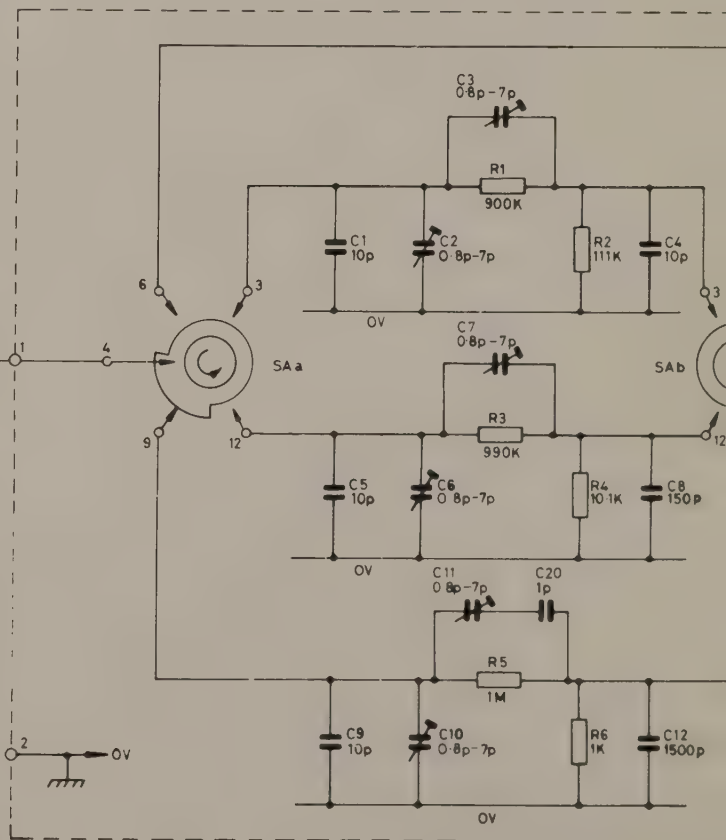




V/cm SELECTED	WAFER CONTACTS MADE			
	SAa	SAb	SAc	SAd
50	9	9	2	3
20	9	9	6	7
10	12	12	10	11
5	12	12	2	3
2	12	12	6	7
1	3	3	10	11
0·5	3	3	2	3
0·2	3	3	6	7
0·1	6	6	10	11
0·05	6	6	2	3
0·02	6	6	6	7

V/cm SWITCHES WAFER CONTACTS MADE ON THE SELECTED ATTENUATIONS





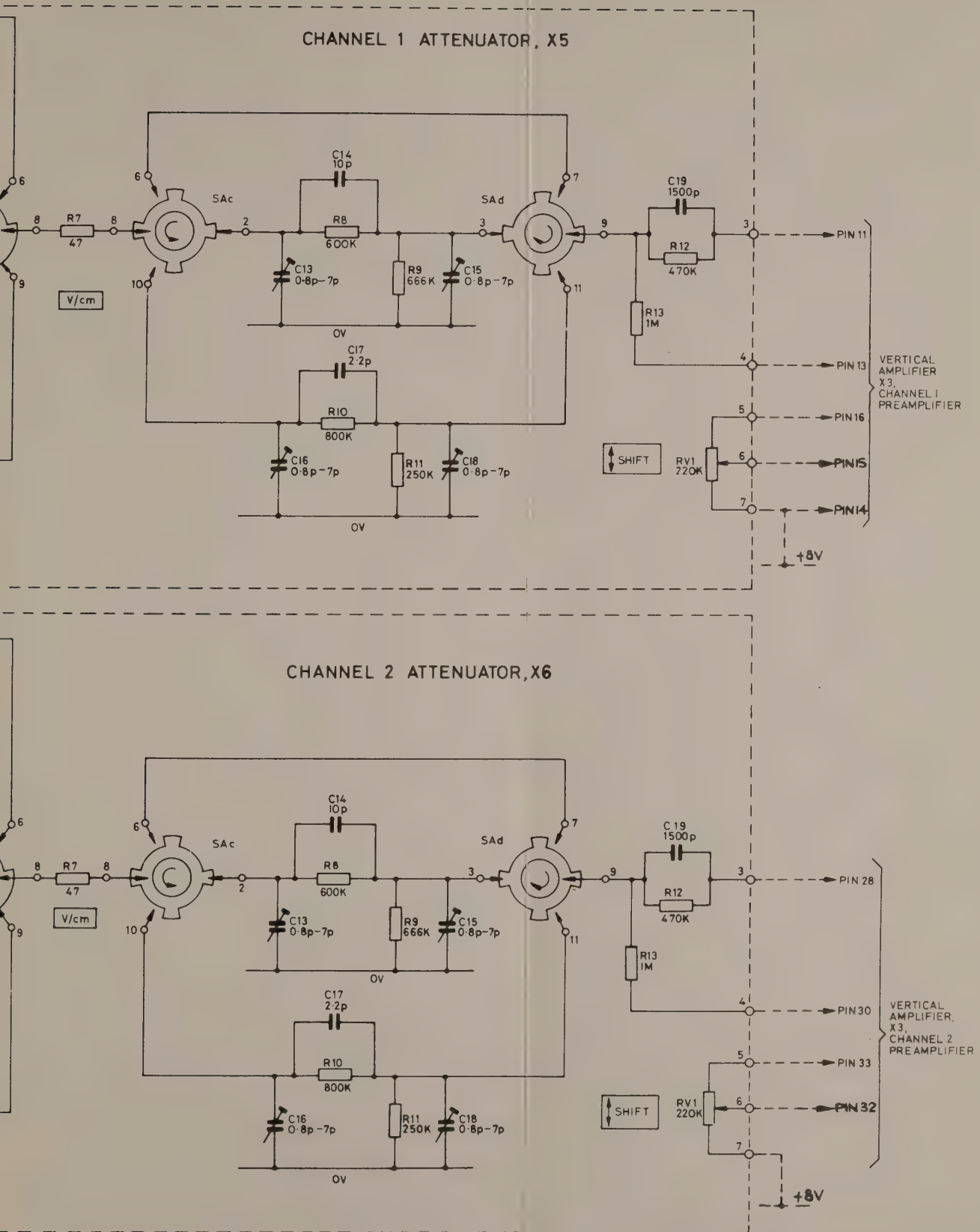


Fig. 7.6 Attenuators X5 and X6 (Channel 1 and 2)
Circuit Diagram

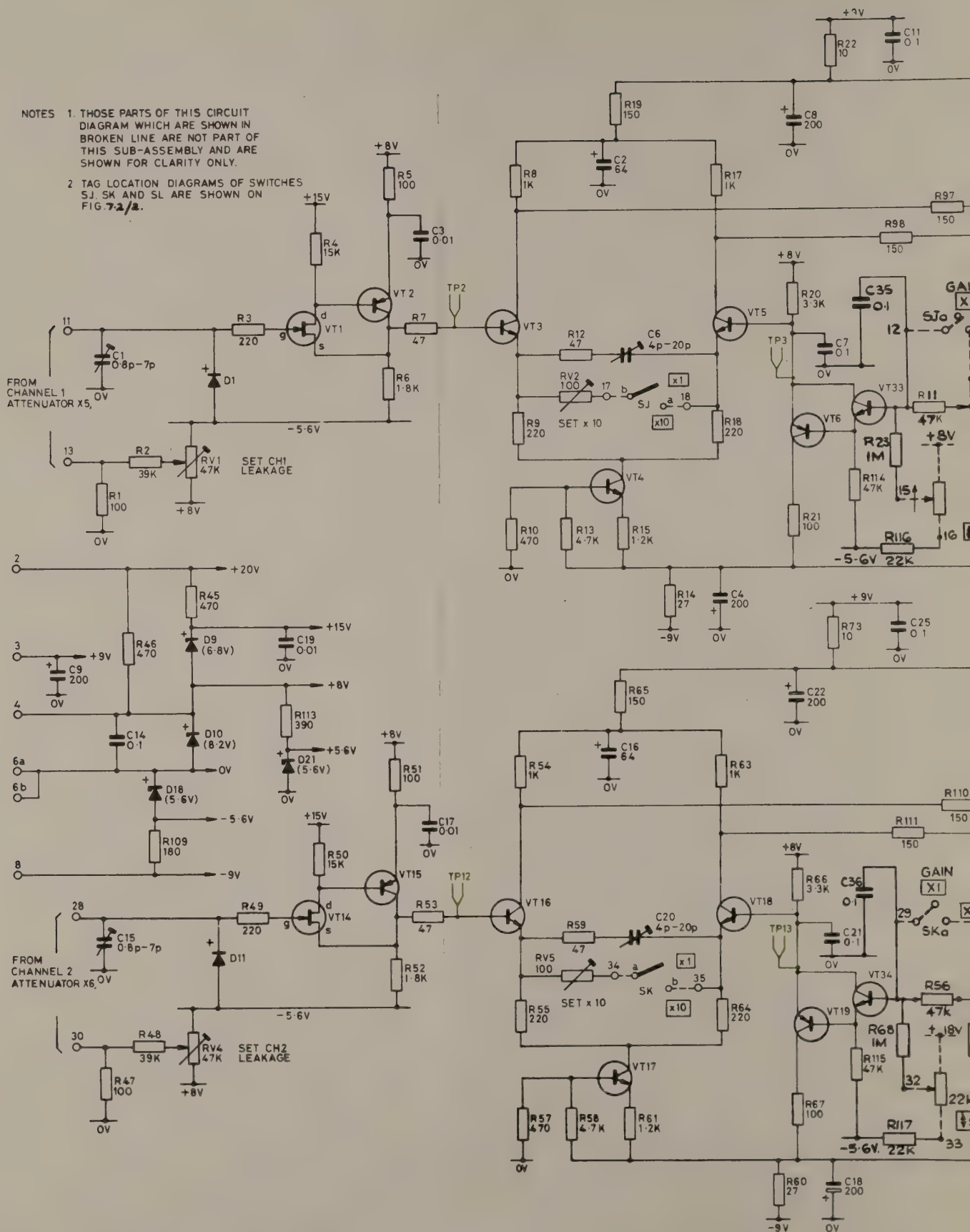
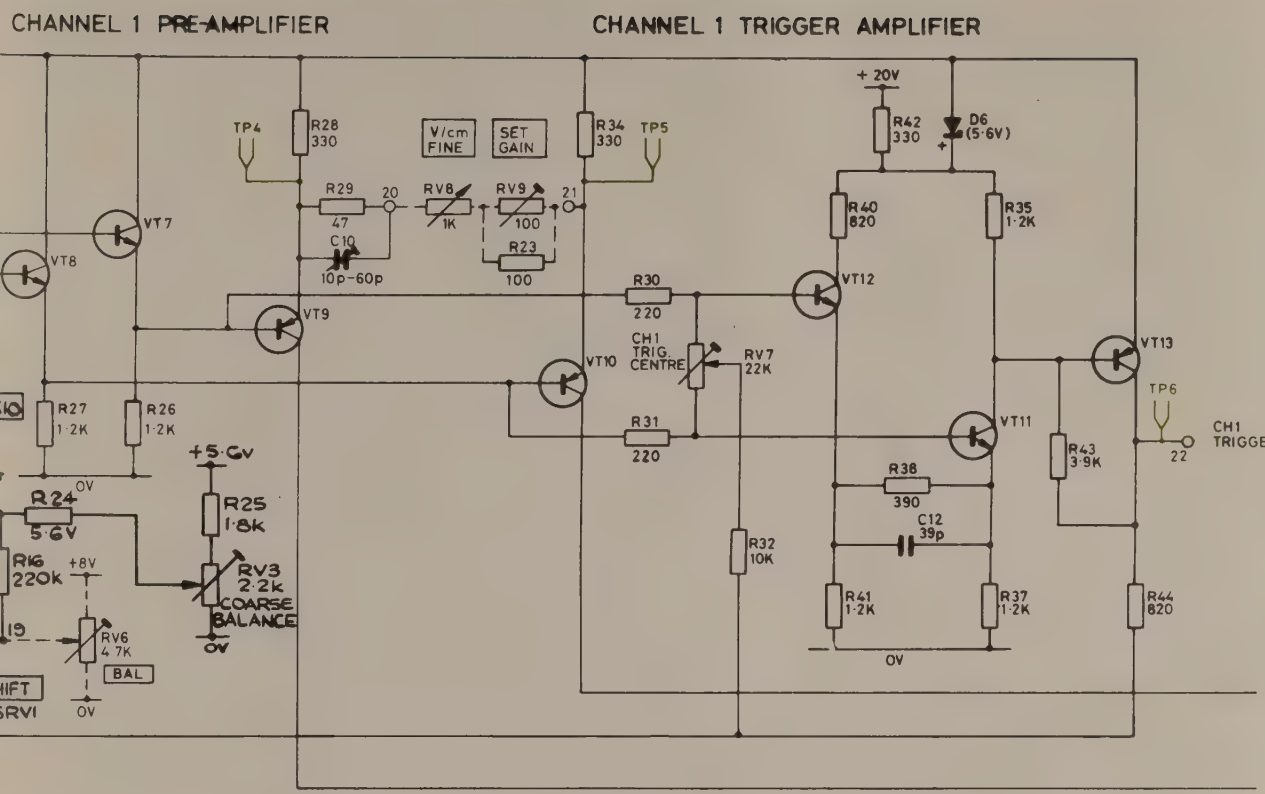
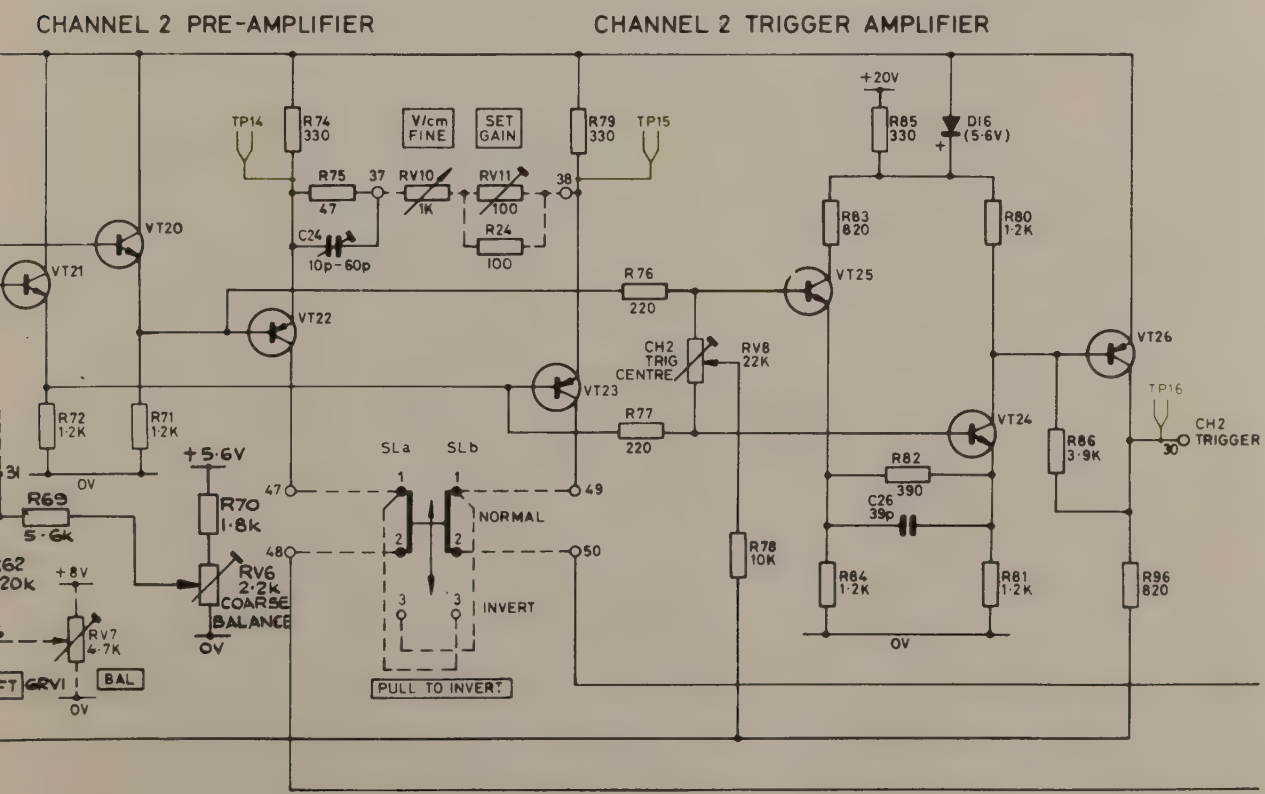
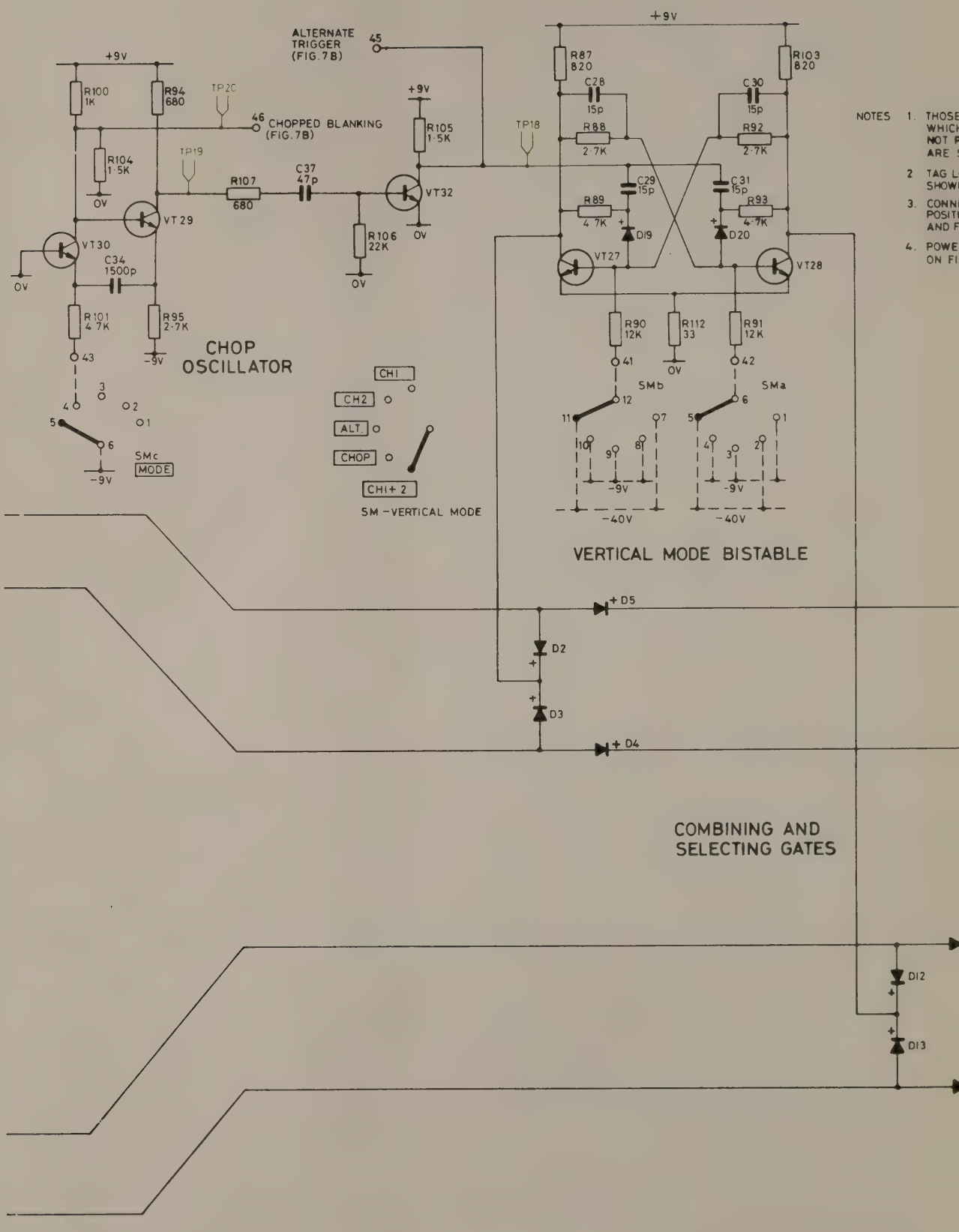

NOTES 1. THOSE PARTS OF THIS CIRCUIT DIAGRAM WHICH ARE SHOWN IN BROKEN LINE ARE NOT PART OF THIS SUB-ASSEMBLY AND ARE SHOWN FOR CLARITY ONLY.
2 TAG LOCATION DIAGRAMS OF SWITCHES SJ, SK AND SL ARE SHOWN ON FIG. 7.2/2.
FROM CHANNEL 1 ATTENUATOR X5,
FROM CHANNEL 2 ATTENUATOR X6,
SET CH1 LEAKAGE
SET CH2 LEAKAGE
SET x 10
GAIN
+20V
+15V
+8V
+9V
+5·6V
-5·6V
-9V
0V

Fig. 7.7 Y Amplifier X3 Circuit Diagram


CHANNEL 1 PRE-AMPLIFIER
CHANNEL 1 TRIGGER AMPLIFIER
TP4
R28 330
V/cm FINE
SET GAIN
R34 330
TP5
+20V
R42 330
D6 (5·6V)
R29 47
20
RV8 1K
RV9 100
21
R23 100
C10 10p-60p
R40 820
R35 1·2K
VT7
VT8
VT9
R30 220
VT12
CH1 TRIG CENTRE
RV7 22K
VT10
VT13
TP6
CH1 TRIGGER
22
R27 1·2K
R26 1·2K
R31 220
VT11
R43 3·9K
+5·6V
R25 1·8K
R24 5·6K
R38 390
C12 39p
R32 10K
R16 220K
+8V
RV3 2·2K COARSE BALANCE
RV6 4·7K
BAL
R41 1·2K
R37 1·2K
R44 820
0V


CHANNEL 2 PRE-AMPLIFIER
CHANNEL 2 TRIGGER AMPLIFIER
TP14
R74 330
V/cm FINE
SET GAIN
R79 330
TP15
+20V
R85 330
D16 (5·6V)
R75 47
37
RV10 1K
RV11 100
38
R24 100
C24 10p-60p
R83 820
R80 1·2K
VT20
VT21
VT22
R76 220
VT25
CH2 TRIG CENTRE
RV8 22K
VT23
VT26
TP16
CH2 TRIGGER
30
R72 1·2K
R71 1·2K
R77 220
VT24
R86 3·9K
+5·6V
SLa
SLb
R82 390
C26 39p
R69 5·6K
R70 1·8K
47
49
NORMAL
48
50
R78 10K
RV6 2·2K COARSE BALANCE
INVERT
R84 1·2K
R81 1·2K
R96 820
RV7 4·7K
BAL
PULL TO INVERT
0V


+9V
ALTERNATE TRIGGER (FIG.7B)
45
R100 1K
R94 680
TP20
46 CHOPPED BLANKING (FIG.7B)
R104 1·5K
TP19
R107 680
C37 47p
R105 1·5K
TP18
R106 22K
VT29
VT30
VT32
C34 1500p
R101 4·7K
R95 2·7K
43
CHOP OSCILLATOR
SMc
MODE
CH1
CH2
ALT.
CHOP
CH1+2
SM – VERTICAL MODE
R87 820
R103 820
C28 15p
C30 15p
R88 2·7K
R92 2·7K
C29 15p
C31 15p
R89 4·7K
R93 4·7K
D19
D20
VT27
VT28
R90 12K
R112 33
R91 12K
41
42
SMb
SMa
VERTICAL MODE BISTABLE
-40V
D5
D2
D3
D4
COMBINING AND SELECTING GATES
D12
D13
NOTES 1. THOSE WHICH NOT F ARE S
2 TAG L SHOWI
3. CONNI POSITI AND F
4. POWE ON FI

PARTS OF THIS CIRCUIT DIAGRAM
ARE SHOWN IN BROKEN LINE ARE
RT OF THESE SUB-ASSEMBLIES AND
HOWN FOR CLARITY ONLY.

CATION DIAGRAMS OF SWITCH SM ARE
ON FIG. 3B.

CTIONS TO THE 'CHOP' AND 'ALT'
NS OF SMd ARE SHOWN ON FIG. 7A.
.7B. RESPECTIVELY.

SUPPLY CONNECTIONS ARE SHOWN
. 12A.

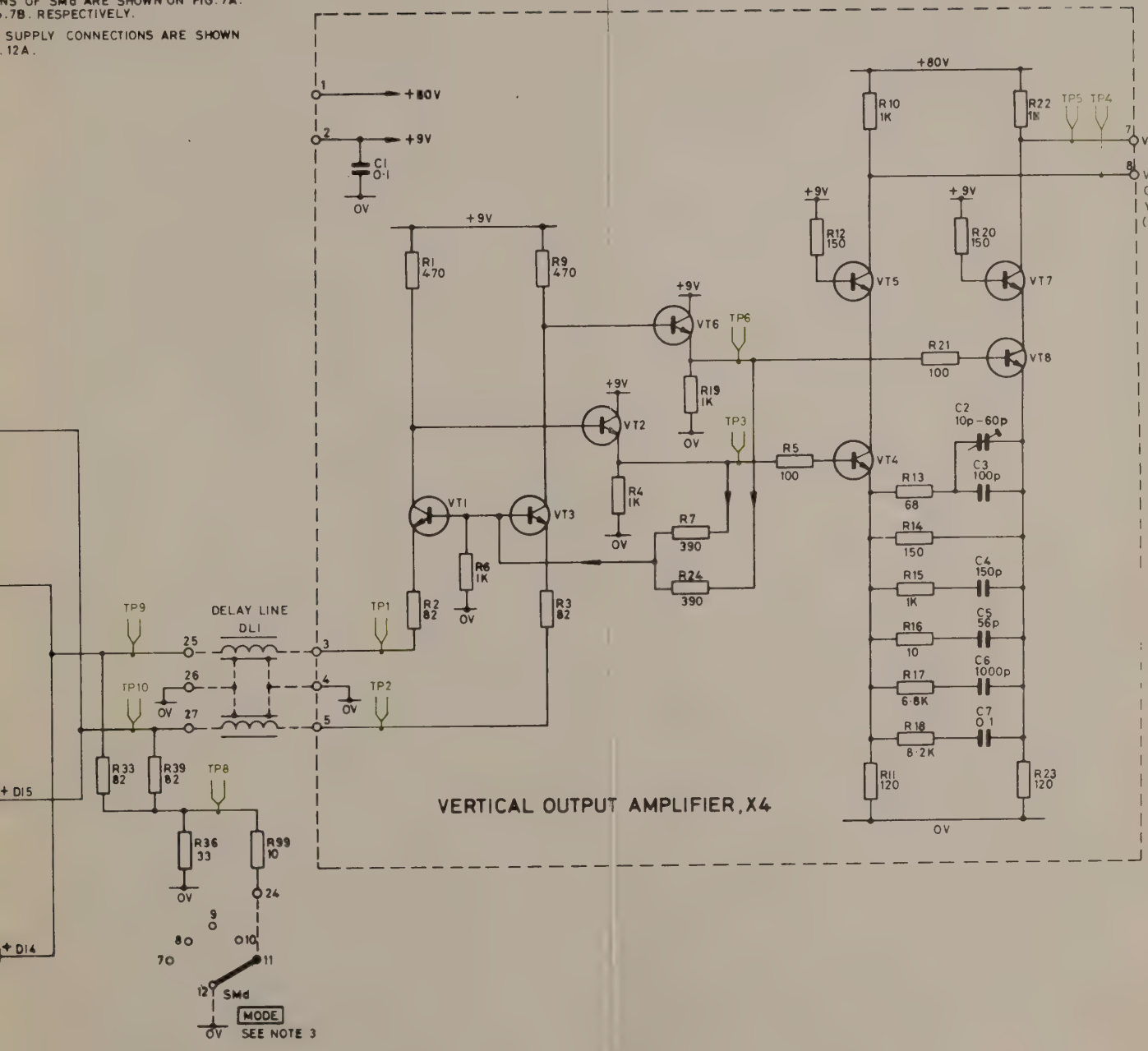


Fig. 7|8 Y Amplifier X3 - Mode Selector Circuit Diagram
Y Output Amplifier X4 Circuit Diagram

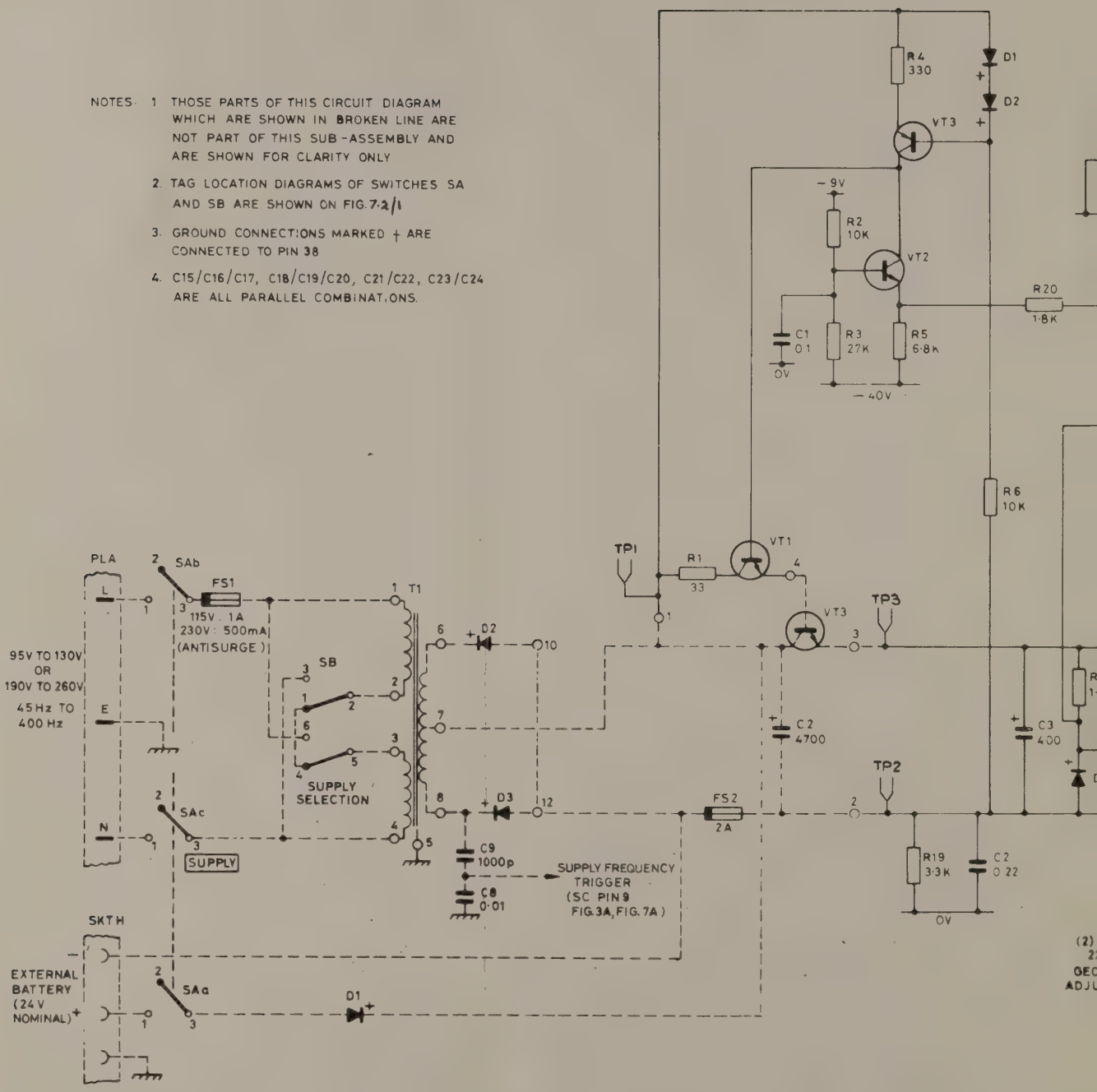
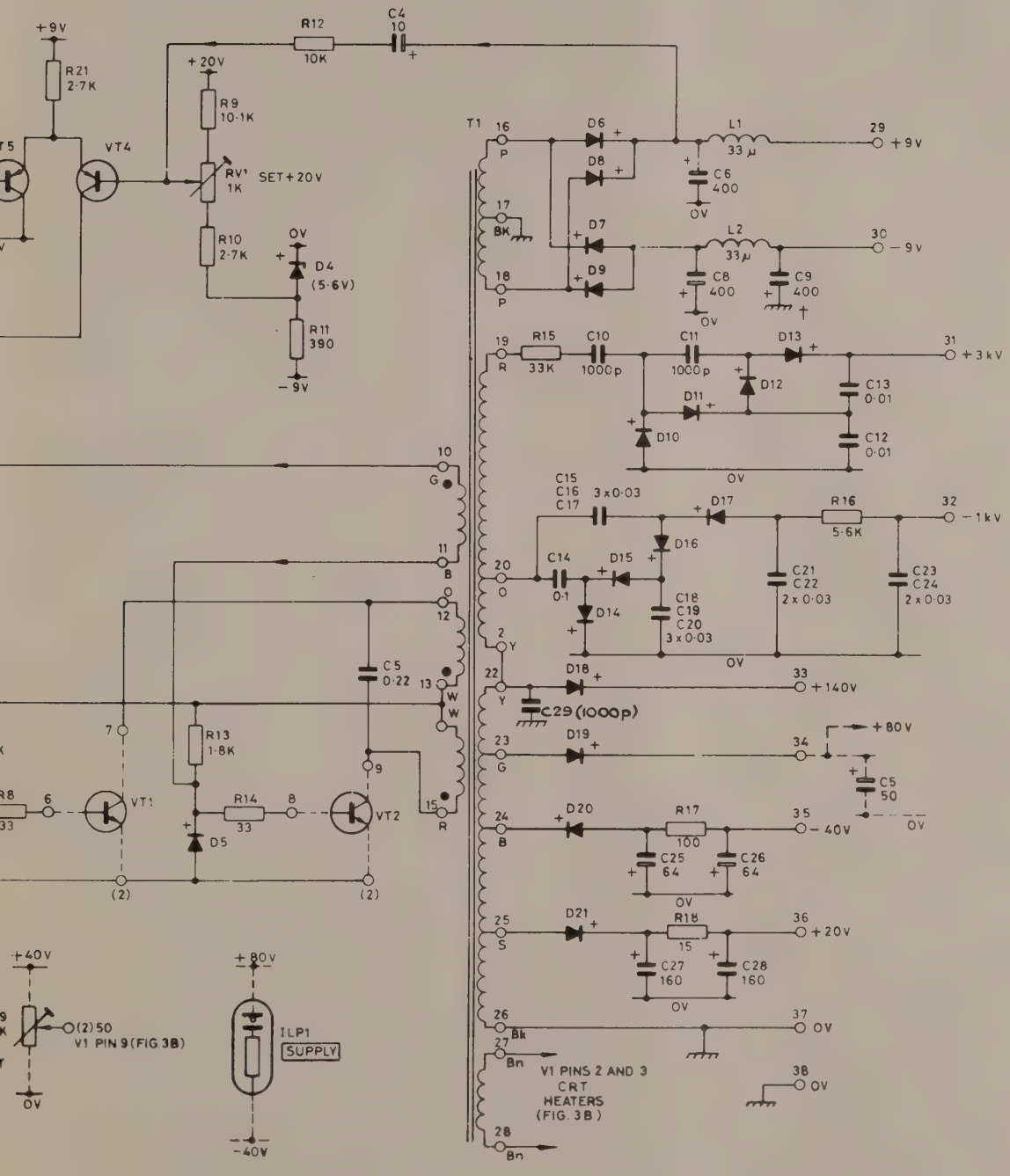


Fig. 7.9 Power Supply Unit (TF 2204) Circuit Diagram


+9V
R21 2·7K
+20V
R9 10·1K
RV1 1K
SET +20V
R10 2·7K
D4 (5·6V)
R11 390
-9V
R12 10K
C4 10
VT4
VT5
T1
D6
D8
D7
D9
L1 33 µ
L2 33µ
C6 400
C8 400
C9 400
+9V
-9V
R15 33K
C10 1000p
C11 1000p
D13
D12
D11
D10
C13 0·01
C12 0·01
+3kV
C15 C16 C17 3x0·03
D17
R16 5·6K
-1kV
D16
D15
C14 0·1
D14
C18 C19 C20 3x0·03
C21 C22 2x0·03
C23 C24 2x0·03
D18
+140V
C29 (1000p)
C5 0·22
R13 1·8K
R14 33
D5
VT1
VT2
+80V
C5 50
D19
D20
R17 100
-40V
C25 64
C26 64
D21
R18 15
+20V
C27 160
C28 160
OV
V1 PINS 2 AND 3 CRT HEATERS (FIG. 3B)
+40V
(2) 50
V1 PIN 9 (FIG. 3B)
+80V
ILP1
SUPPLY
-40V

The voltage source circuit of the TF2204 (shown in the broken line in Fig. 7.9) is replaced by this circuit in the TF2204/1.

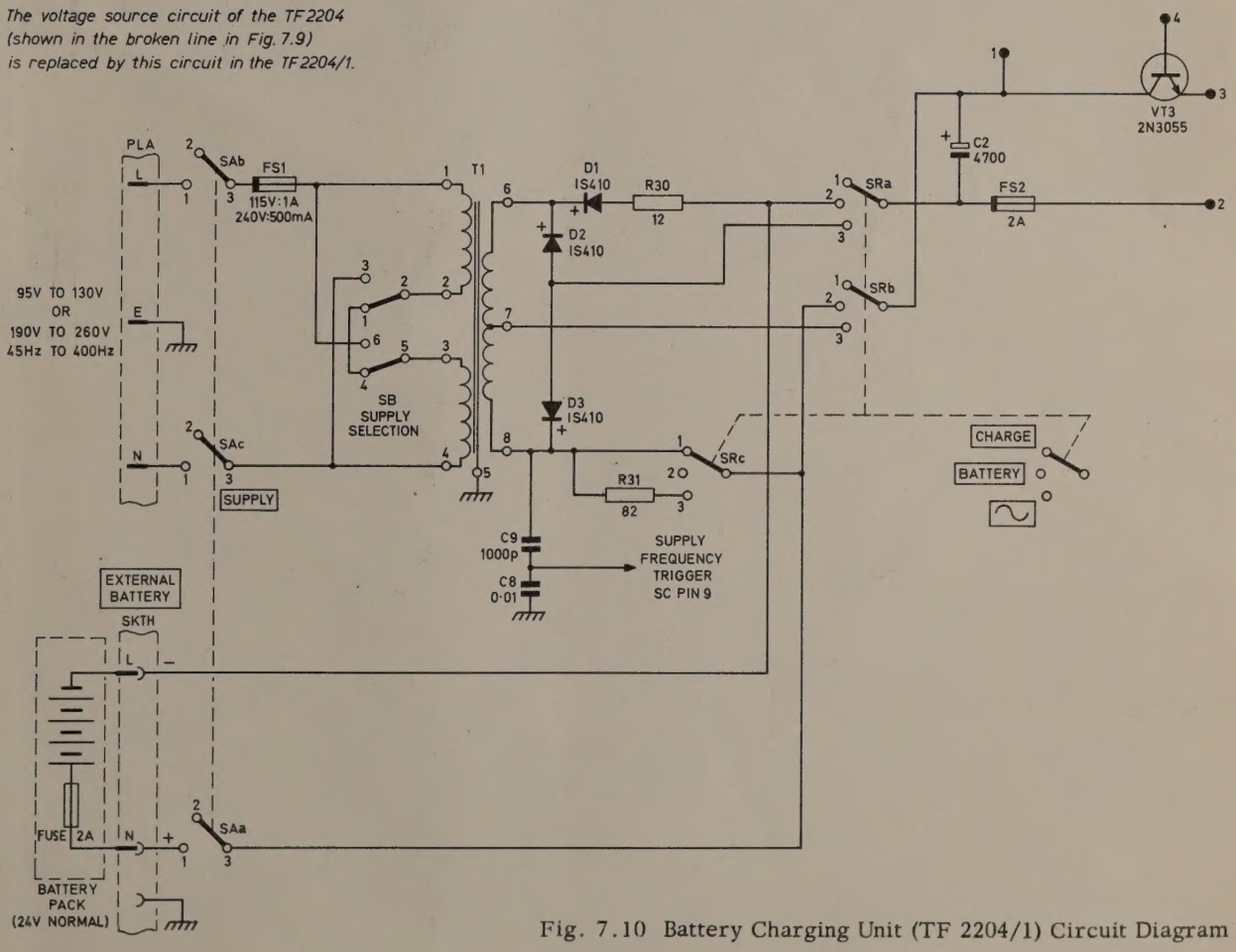


Fig. 7.10 Battery Charging Unit (TF 2204/1) Circuit Diagram

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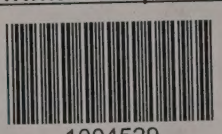

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